Single-Photon Avalanche Diodes in CMOS Technology: Towards Low-Cost and Compact Solid-State LiDAR Sensors

(Invited Review Paper)

Myung-Jae Lee
Korea Institute of Science and Technology (KIST), 5, Hwarang-ro 14-gil, Seongbuk-gu, Seoul 02792, Republic of Korea
Author e-mail address: mj.lee@kist.re.kr

Abstract: The goal of this paper is to introduce single-photon avalanche diodes (SPADs) in CMOS technology, which are getting a lot of attention especially from the industry to realize low-cost and compact solid-state LiDAR sensors.

1. Introduction

Single-photon avalanche diodes (SPADs) generate extremely large internal gain enabling single-photon detection owing to impact-ionization effect, also known as the avalanche multiplication process. In addition, they also provide accurate photon counting and time-of-arrival detection with the digital nature of their output. Also, as solid-state devices, SPADs have advantages in terms of size, scalability, and price compared to photomultiplier tubes (PMTs) and micro-channel plates (MCPs). The implementation of SPADs in standard CMOS technology has enabled monolithic integration with electronic circuits, opening the way to compact, low-cost, and high-volume fabrication. Therefore, CMOS SPADs become a very promising solution in order to realize next-generation light detection and ranging (LiDAR) sensors (i.e., low-cost and compact solid-state LiDAR sensors) so that they are recently getting a lot of attention, especially from the industry for autonomous vehicles. Another emerging field requiring the CMOS-SPAD technology as a major attraction for industry is direct time-of-flight (D-ToF) sensor applications (e.g., face and/or gesture recognition in mobile phones) due to the fact that SPAD-based D-ToF sensors can greatly increase the detection range, which is currently limited by the efficiency of CMOS photodiodes (PDs) used in indirect ToF (I-ToF) sensors. Besides, SPADs are also very useful in many biomedical applications such as time-of-flight positron emission tomography (TOF PET), fluorescence-lifetime imaging microscopy (FLIM), super-resolution microscopy, near-infrared imaging (NIRI), etc. and quantum applications like quantum key distribution (QKD), quantum random number generators (QRNG), optical quantum computing, etc. [1–3]. This paper will provide an overview and recent R&D progress of the SPAD, and then a brief outlook on the future of the SPAD will conclude the paper.

2. CMOS SPADs: Overview and Recent R&D Progress

A common CMOS-SPAD structure based on P^+/N-well junction and P-well guard ring (GR) is shown in Fig. 1(a). Unlike a PD, a SPAD requires a GR structure to prevent premature breakdown at the edge of the junction caused by junction-curvature effect [4]. Its operation process is described in Fig. 1(b): (1) when one applies higher reverse bias voltage to a SPAD than its breakdown voltage, the avalanche multiplication process starts if an injected photon generates an electron-hole pair, (2) the bias across the SPAD is decreased below its breakdown voltage by the large

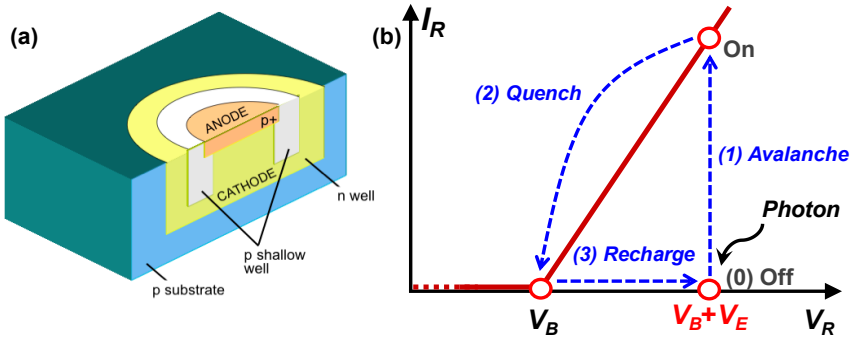

Fig. 1. (a) Cross-section of a SPAD fabricated in standard CMOS technology and (b) SPAD operation process.

current generated by the avalanche process and a high resistor connected to its output called quenching resistor, and (3) it is recharged to the initial voltage condition to detect another photon [3].

A SPAD is mainly characterized in terms of (i) dark count rate (DCR): the rate of spurious pulses due to thermal generation, trap-assisted thermal generation, trap-assisted tunneling, and band-to-band tunneling, (ii) photon detection probability (PDP): probability that an injected photon triggers a pulse, (iii) timing jitter: uncertainty between actual and measured photon arrival time, (iv) afterpulsing probability (APP): probability that an avalanche causes false counts due to traps, and (v) fill factor (FF): ratio of photon-sensitive area to total area [3].

Among the SPAD characteristics, the most critical factor is efficiency (i.e., PDP and FF) for LiDAR and ToF applications using near-infrared (NIR) wavelengths (e.g., 850, 905, 940nm) because CMOS SPADs suffer from low PDP at NIR due to shallow and highly-doped junctions in CMOS and also low FF owing to surrounding GR and pixel circuits as shown in Fig. 2. In order to solve the issues, using better CMOS technology for SPADs (e.g., CMOS image sensor (CIS), high-voltage (HV) CMOS, bipolar-CMOS-DMOS (BCD) which provide deeper and lowly-doped layers) is essential to increase the PDP at the long wavelength. In addition, emerging 3D CMOS technology is a very useful technology for SPADs in order to improve FF as shown in Fig. 2(b). Since the area increases not only for SPADs but also circuits, it enables more functionality per pixel so that improves overall sensor performance [5–7].

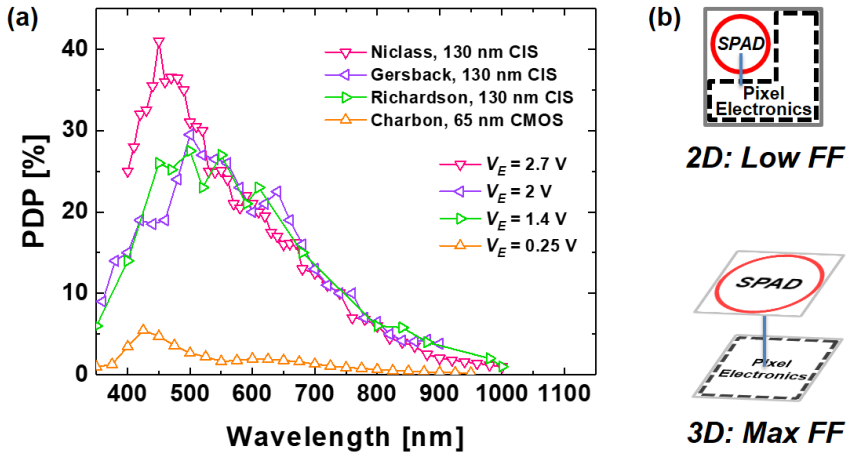

Fig. 2. (a) Examples of PDP characteristics of SPADs in advanced CMOS technologies below 130nm and (b) fill-factor comparison between 2D and 3D approaches.

3. Conclusions

CMOS SPADs have created a paradigm shift, especially in LiDAR and ToF applications. Although PDP performance of them is in general below 10% at NIR, they can provide capability to enable long-range detection over 100m. It is expected that next-generation CMOS SPADs optimized for NIR applications will guarantee much higher performance for future solid-state LiDAR sensors.

4. References

[1] E. Charbon, "Single-photon imaging in complementary metal oxide semiconductor processes," Phil. Trans. R. Soc. A **372**, 20130100 (2014).
[2] C. Bruschini *et al.*, "Ten years of biophotonics single-photon SPAD imager applications - retrospective and outlook," Proc. SPIE **10069**, 100691S (2017).
[3] M.-J. Lee *et al.*, "CMOS-based single-photon detectors: technology and applications," Opto-Electron. and Commun. Conf. (2018).
[4] M.-J. Lee *et al.*, "Effects of guard-ring structures on the performance of silicon avalanche photodetectors fabricated with standard CMOS technology," IEEE Electron Device Lett. **33**, 80 (2012).
[5] M.-J. Lee *et al.*, "A back-illuminated 3D-stacked single-photon avalanche diode in 45nm CMOS technology," Int. Electron Devices Meeting (2017).
[6] M.-J. Lee *et al.*, "High-performance back-illuminated three-dimensional stacked single-photon avalanche diode implemented in 45-nm CMOS technology," IEEE J. Sel. Top. Quantum Electron. **24**, 3801809 (2018).
[7] M.-J. Lee and E. Charbon, "Progress in single-photon avalanche diode image sensors in standard CMOS: from two-dimensional monolithic to three-dimensional-stacked technology," Jpn. J. Appl. Phys. **57**, 1002A3 (2018).